Replacement Claims

WHAT IS CLAIMED IS:

1. A bond pad structure in a semiconductor device, comprising:

a first bond pad and a second bond pad; each of the bond pads comprising at least a lower metal layer and an upper metal layer; with a lower metal layer of one of the bond pads extending underneath the upper metal layer of the other of the bond pads.

2. The bond pad structure of Claim 1, wherein the extension of the lower metal layer of the one of the bond pads functions as an etch block to prevent etching of a dielectric layer between the first and second bond pads to a substrate underlying the bond pads.

3. The bond pad structure of Claim 1, wherein the first and second bond pads each comprise a plurality of lower metal layers wherein at least one of the lower metal layers of the one of the bond pads extends underneath the upper metal layer of the other of the bond pads.

A1 4. (amended) The bond pad structure of Claim 3, wherein at least two lower metal layers of the one of the bond pads extend underneath the upper metal layer of the other of the bond pads.

5. The bond pad structure of Claim 1, further comprising a conductive material interconnecting the first bond pad to the second bond pad.

6. The bond pad structure of Claim 5, wherein the conductive material comprises a solder material.

7. The bond pad structure of Claim 5, wherein the conductive material overlies at least a portion of each of the first and second bond pads.

8. The bond pad structure of Claim 5, further comprising a bonding wire connected to the conductive material.

Replacement Claims

9. A bond pad structure in a semiconductor device, comprising:

a first bond pad and a second bond pad; each of the bond pads comprising at least a lower metal layer and an upper metal layer; with a lower metal layer of one of the bond pads extending underneath the upper metal layer of the other of the bond pads; wherein the extension of the lower metal layer of the one of the bond pads functions as an etch block to prevent etching of a dielectric layer between the first and second bond pads to a substrate underlying the bond pads.

10. The bond pad structure of Claim 9, further comprising a conductive material interconnecting and overlying at least a portion of the first and second bond pads.

11. A bond pad structure in a semiconductor device, comprising:

a first bond pad and a second bond pad; each of the bond pads comprising at least a lower metal layer and an upper metal layer; with a lower metal layer of the first bond pad extending beneath the upper metal layer of the second bond pad.

12. A bond pad structure in a semiconductor device, comprising:

a first bond pad and a second bond pad; each of the bond pads comprising at least a lower metal layer and an upper metal layer; with a lower metal layer of the second bond pad extending beneath the upper metal layer of the first bond pad.

13. A bond pad structure in a semiconductor device, comprising:

a first bond pad interconnected to a second bond pad by a conductive material; each of the bond pads comprising at least a lower metal layer and an upper metal layer; with a lower metal layer of one of the bond pads extending underneath the upper metal layer of the other of the bond pads.

14. The bond pad structure of Claim 13, wherein the conductive material overlies a portion of each of the bond pads.

15. The bond pad structure of Claim 13, wherein the conductive material comprises a solder material.

16. The bond pad structure of Claim 13, further comprising a bonding wire connected to the conductive material.

17. The bond pad structure of Claim 13, wherein the extension of the lower metal layer of the one of the bond pads functions as an etch block to prevent etching of a dielectric material between the first and second bond pads to a substrate underlying the bond pads.

18. A bond pad structure in a semiconductor device, comprising:

a first bond pad and a second bond pad positioned within a single passivation opening; the first and second bond pads interconnected by a conductive material overlying at least a portion of each of the bond pads; and each of the bond pads comprising at least a lower metal layer and an upper metal layer; with a lower metal layer of one of the bond pads extending underneath the upper metal layer of the other of the bond pads.

19. The bond pad structure of Claim 18, further comprising a passivation layer overlying a portion of each of the bond pads, the opening being formed through the passivation layer to expose the bond pads.

20. The bond pad structure of Claim 18, wherein the conductive material comprises solder.

21. The bond pad structure of Claim 18, further comprising a bonding wire connected to the conductive material.

22. (amended) A bond pad structure in a semiconductor device, comprising:

A2

a first metal layer deposited onto a substrate and patterned to form first and second lower metal layer portions having a space thereinbetween;

a dielectric layer deposited over the first and second lower metal layer portions and the substrate within the space, and etched to form openings to each of the first and second lower metal layer portions; and

a second metal layer deposited over the dielectric layer and into the openings of the dielectric layer and etched to form a first and second upper metal layer portions overlying and in conductive contact with the first and second lower metal layer portions; the first upper and lower metal layer portions forming a first bond pad, and the second upper and lower metal layer portions forming a second bond pad;

wherein a lower metal layer portion of one of the bond pads extends beneath the upper metal layer portion of the other of the bond pads.

23. The bond pad structure of Claim 22, further comprising a passivation layer formed over the bond pads and etched to form an opening therethrough to expose the first and second bond pads.

24. The bond pad structure of Claim 22, further comprising a conductive material interconnecting the first bond pad to the second bond pad.

25. The bond pad structure of Claim 24, wherein the conductive material comprises a solder material.

26. The bond pad structure of Claim 24, wherein the conductive material overlies at least a portion of each of the first and second bond pads.

27. The bond pad structure of Claim 24, further comprising a bonding wire connected to the conductive material.

28. A bond pad structure in a semiconductor device, comprising:

a first bond pad and a second bond pad; each of the bond pads comprising at least a lower metal layer and an upper metal layer; with a lower metal layer of one of the bond pads extending beneath the upper metal layer of the other of the bond pads; and

at least one of the bond pads functions to supply data, retrieve data, test a device, or supply various voltage levels.

29. The bond pad structure of Claim 28, wherein the first bond pad is functional to receive and respond to a test mode signal by entering a test mode; and upon discontinuing the test mode and being interconnected to the second bond pad, the first and second bond pads are functional to a receive and respond to operational mode signals.

30. The bond pad structure of Claim 29, wherein the lower metal layer of the first bond pad extends beneath the upper metal layer of the second bond pad.

31. The bond pad structure of Claim 29, wherein the lower metal layer of the second bond pad extends beneath the upper metal layer of the first bond pad.

32. A bond pad structure in a semiconductor device, comprising:

a first bond pad and a second bond pad; each of the first and second bond pads comprising at least a lower metal layer and an upper metal layer; with a lower metal layer of one of the bond pads extending underneath the upper metal layer of the other of the bond pads; and

the first bond pad functional to receive and respond to a test mode signal by entering a test mode; and upon discontinuing the test mode and being interconnected to the second bond pad, the first and second bond pads functional to a receive and respond to an operational mode signals by entering an operational mode.

33. The bond pad structure of Claim 32, wherein the lower metal layer of the first bond pad extends underneath the upper metal layer of the second bond pad.

34. The bond pad structure of Claim 32, wherein the lower metal layer of the second bond pad extends underneath the upper metal layer of the first bond pad.

50. An integrated circuit die, comprising:

a first bond pad and a second bond pad, the first and second bond pads being positioned within a single passivation opening; each of the first and second bond pads comprising at least a lower metal layer and an upper metal layer; with a lower metal layer of one of the bond pads extending underneath the upper metal layer of the other of the bond pads.

51. The integrated circuit die of Claim 50, wherein the lower metal layer of the first bond pad extends underneath the upper metal layer of the second bond pad.

52. The integrated circuit die of Claim 50, wherein the lower metal layer of the second bond pad extends underneath the upper metal layer of the first bond pad.

53. The integrated circuit die of Claim 50, further comprising a conductive material interconnecting and overlying at least a portion of the first bond pad and the second bond pad.

54. The integrated circuit die of Claim 53, wherein the conductive material comprises solder.

55. The integrated circuit die of Claim 53, further comprising a bonding wire connected to at least one of the bond pads.

56. The integrated circuit die of Claim 50, wherein the first and second bond pads each comprise a plurality of lower metal layers wherein at least two lower metal layer of the one of the bond pads extend underneath the upper metal layer of the other of the bond pads.

57. The integrated circuit die of Claim 50, wherein the extension of the lower metal layer of the one of the bond pads functions as an etch block to prevent etching of a dielectric material between the first and second bond pads to a substrate underlying the bond pads.

58. An integrated circuit die, comprising:

a first bond pad interconnected to a second bond pad, the first and second bond pads being positioned within a single passivation opening;

each of the first and second bond pads comprising at least a lower metal layer and an upper metal layer; with a lower metal layer of one of the bond pads extending beneath the upper metal layer of the other of the bond pads; wherein the extension of the lower metal layer of the one of the bond pads functions as an etch block to prevent etching of a dielectric layer between the first and second bond pads to a substrate underlying the bond pads.

59. The integrated circuit die of Claim 58, wherein the first and second bond pads are interconnected by a conductive material interconnecting overlying and in conductive contact with at least a portion of each of the bond pads.

60. An integrated circuit die, comprising:

a first bond pad interconnected to a second bond pad, the first and second bond pads being positioned within a single passivation opening; each of the first and second bond pads comprising at least a lower metal layer and an upper metal layer; and the lower metal layer of the first bond pad extending beneath the upper metal layer of the second bond pad.

61. An integrated circuit die, comprising:

a first bond pad interconnected to a second bond pad, the first and second bond pads being positioned within a single passivation opening; each of the first and second bond pads comprising at least a lower metal layer and an upper metal layer; with the lower metal layer of the second bond pad extending beneath the upper metal layer of the first bond pad.

62. An integrated circuit die, comprising:

a first bond pad and a second bond pad; each of the first and second bond pads comprising at least a lower metal layer and an upper metal layer; the lower metal layer of one of the bond pads extending beneath the upper metal layer of the other of the bond pads; and at least one of the bond pads functional to supply data, retrieve data, test a device, or supply various voltages.

63. The integrated circuit die of Claim 62, further comprising a conductive material interconnecting and overlying at least a portion of each of the bond pads.

64. The integrated circuit die of Claim 62, wherein the first bond pad is functional to receive and respond to a test mode signal by entering a test mode, and upon discontinuing the test mode and being interconnected to the second bond pad, the first and second bond pads are functional to receive and respond to an operational mode signal by entering an operational mode.

65. The integrated circuit die of Claim 64, further comprising a conductive material interconnecting and overlying at least a portion of each of the bond pads.

A3

69. (new) A bond pad structure disposed on a substrate and comprising multiple bond pads, each bond pad comprising overlying upper and lower metal layers, and the upper metal layer of one of the bond pads overlapping the lower metal layer of another of the bond pads.

A3

70. (new) A bond pad structure disposed on a substrate and comprising two or more bond pads, each bond pad comprising overlying upper and lower metal layers, and the upper metal layer of one of the bond pads extending over the lower metal layer of another of the bond pads.

71. (new) A bond pad structure disposed on a substrate and comprising:

a lower metal layer disposed on the substrate and comprising first and second portions separated by a space therebetween;

a dielectric layer overlying the lower metal layer and the substrate within the space; one or more openings extending through the dielectric layer to each of the first and second lower metal portions; and

an upper metal layer disposed over the dielectric layer and within the openings in the dielectric layer in contact with the first and second portions of the lower metal layer; the upper metal layer comprising first and second portions, the first upper metal portion positioned over the first lower metal portion to form a first bond pad, and the second upper metal portion positioned over the second lower metal portion to form a second bond pad; and the upper metal portion of one of the bond pads extends over the lower metal portion of the other bond pad.

72. (new) An integrated circuit supported by a substrate and comprising: a bond pad structure, the bond pad structure comprising two or more bond pads, each bond pad comprising overlying upper and lower metal layers, and the upper metal layer of one of the bond pads extending over the lower metal layer of another of the bond pads.

73. (new) An integrated circuit supported by a substrate and comprising: a first bond pad and a second bond pad; each of the bond pads comprising a lower metal layer and an overlying upper metal layer; and the upper metal layer of one of the bond pads extends beyond the lower metal layer of the one bond pad and over the lower metal layer of the other of the bond pads.

A3

74. (new) An integrated circuit supported by a substrate and comprising a bond pad structure, the bond pad structure comprising:

a lower metal layer comprising first and second portions with a space therebetween;

a dielectric layer overlying the lower metal layer and within the space; at least one opening extending through the dielectric layer to each of the first and second lower metal portions; and

an upper metal layer overlying the dielectric layer and within the openings in the dielectric layer in contact with the first and second portions of the lower metal layer; the upper metal layer comprising first and second portions, the first upper metal portion positioned over the first lower metal portion to form a first bond pad, and the second upper metal portion positioned over the second lower metal portion to form a second bond pad; and the upper metal portion of one of the bond pads extends over the lower metal portion of the other bond pad.

75. (new) A semiconductor device, comprising:

a substrate; and

a bond pad structure disposed on the substrate, the bond pad structure comprising multiple bond pads, each bond pad comprising overlying upper and lower metal layers, and the upper metal layer of one of the bond pads overlaps the lower metal layer of another of the bond pads.

76. (new) A semiconductor wafer, comprising:

a substrate and a bond pad structure disposed on the substrate, the bond pad structure comprising a first bond pad and a second bond pad; each of the bond pads comprising a lower metal layer and an overlying upper metal layer; and the upper metal layer of one of the bond pads extends beyond the lower metal layer of the one bond pad and over the lower metal layer of the other of the bond pads.

WHAT IS CLAIMED IS:

1. A bond pad structure in a semiconductor device, comprising:

a first bond pad and a second bond pad; each of the bond pads comprising at least a lower metal layer and an upper metal layer; with a lower metal layer of one of the bond pads extending underneath the upper metal layer of the other of the bond pads.

2. The bond pad structure of Claim 1, wherein the extension of the lower metal layer of the one of the bond pads functions as an etch block to prevent etching of a dielectric layer between the first and second bond pads to a substrate underlying the bond pads.

3. The bond pad structure of Claim 1, wherein the first and second bond pads each comprise a plurality of lower metal layers wherein at least one of the lower metal layers of the one of the bond pads extends underneath the upper metal layer of the other of the bond pads.

4. (amended) The bond pad structure of Claim 3, wherein at least two lower metal layers of the one of the bond pads extend underneath the upper metal layer of the other of the bond pads.

5. The bond pad structure of Claim 1, further comprising a conductive material interconnecting the first bond pad to the second bond pad.

6. The bond pad structure of Claim 5, wherein the conductive material comprises a solder material.

7. The bond pad structure of Claim 5, wherein the conductive material overlies at least a portion of each of the first and second bond pads.

8. The bond pad structure of Claim 5, further comprising a bonding wire connected to the conductive material.

9. A bond pad structure in a semiconductor device, comprising:

a first bond pad and a second bond pad; each of the bond pads comprising at least a lower metal layer and an upper metal layer; with a lower metal layer of one of the bond pads extending underneath the upper metal layer of the other of the bond pads; wherein the extension of the lower metal layer of the one of the bond pads functions as an etch block to prevent etching of a dielectric layer between the first and second bond pads to a substrate underlying the bond pads.

10. The bond pad structure of Claim 9, further comprising a conductive material interconnecting and overlying at least a portion of the first and second bond pads.

11. A bond pad structure in a semiconductor device, comprising:

a first bond pad and a second bond pad; each of the bond pads comprising at least a lower metal layer and an upper metal layer; with a lower metal layer of the first bond pad extending beneath the upper metal layer of the second bond pad.

12. A bond pad structure in a semiconductor device, comprising:

a first bond pad and a second bond pad; each of the bond pads comprising at least a lower metal layer and an upper metal layer; with a lower metal layer of the second bond pad extending beneath the upper metal layer of the first bond pad.

13. A bond pad structure in a semiconductor device, comprising:

a first bond pad interconnected to a second bond pad by a conductive material; each of the bond pads comprising at least a lower metal layer and an upper metal layer; with a lower metal layer of one of the bond pads extending underneath the upper metal layer of the other of the bond pads.

14. The bond pad structure of Claim 13, wherein the conductive material overlies a portion of each of the bond pads.

15. The bond pad structure of Claim 13, wherein the conductive material comprises a solder material.

16. The bond pad structure of Claim 13, further comprising a bonding wire connected to the conductive material.

17. The bond pad structure of Claim 13, wherein the extension of the lower metal layer of the one of the bond pads functions as an etch block to prevent etching of a dielectric material between the first and second bond pads to a substrate underlying the bond pads.

18. A bond pad structure in a semiconductor device, comprising:

a first bond pad and a second bond pad positioned within a single passivation opening; the first and second bond pads interconnected by a conductive material overlying at least a portion of each of the bond pads; and each of the bond pads comprising at least a lower metal layer and an upper metal layer; with a lower metal layer of one of the bond pads extending underneath the upper metal layer of the other of the bond pads.

19. The bond pad structure of Claim 18, further comprising a passivation layer overlying a portion of each of the bond pads, the opening being formed through the passivation layer to expose the bond pads.

20. The bond pad structure of Claim 18, wherein the conductive material comprises solder.

21. The bond pad structure of Claim 18, further comprising a bonding wire connected to the conductive material.

22. (amended) A bond pad structure in a semiconductor device, comprising:

a first metal layer deposited onto a substrate and patterned to form a first and second lower metal layer portions having a space thereinbetween;

a dielectric layer deposited over the first and second lower metal ~~layers~~ layer portions and the substrate within the space, and etched to form openings to each of the first and second lower metal ~~layers~~ layer portions ; and

a second metal layer deposited over the dielectric layer and into the openings of the dielectric layer and etched to form a first and second upper metal layer portions overlying and in conductive contact with the first and second lower metal ~~layers~~ layer portions; the first upper and lower metal ~~layers~~ layer portions forming a first bond pad, and the second upper and lower metal ~~layers~~ layer portions forming a second bond pad;

wherein a lower metal layer portion of one of the bond pads extends beneath the upper metal layer portion of the other of the bond pads.

23. The bond pad structure of Claim 22, further comprising a passivation layer formed over the bond pads and etched to form an opening therethrough to expose the first and second bond pads.

24. The bond pad structure of Claim 22, further comprising a conductive material interconnecting the first bond pad to the second bond pad.

25. The bond pad structure of Claim 24, wherein the conductive material comprises a solder material.

26. The bond pad structure of Claim 24, wherein the conductive material overlies at least a portion of each of the first and second bond pads.

27. The bond pad structure of Claim 24, further comprising a bonding wire connected to the conductive material.

28. A bond pad structure in a semiconductor device, comprising:

a first bond pad and a second bond pad; each of the bond pads comprising at least a lower metal layer and an upper metal layer; with a lower metal layer of one of the bond pads extending beneath the upper metal layer of the other of the bond pads; and

at least one of the bond pads functions to supply data, retrieve data, test a device, or supply various voltage levels.

29. The bond pad structure of Claim 28, wherein the first bond pad is functional to receive and respond to a test mode signal by entering a test mode; and upon discontinuing the test mode and being interconnected to the second bond pad, the first and second bond pads are functional to a receive and respond to operational mode signals.

30. The bond pad structure of Claim 29, wherein the lower metal layer of the first bond pad extends beneath the upper metal layer of the second bond pad.

31. The bond pad structure of Claim 29, wherein the lower metal layer of the second bond pad extends beneath the upper metal layer of the first bond pad.

32. A bond pad structure in a semiconductor device, comprising:

a first bond pad and a second bond pad; each of the first and second bond pads comprising at least a lower metal layer and an upper metal layer; with a lower metal layer of one of the bond pads extending underneath the upper metal layer of the other of the bond pads; and

the first bond pad functional to receive and respond to a test mode signal by entering a test mode; and upon discontinuing the test mode and being interconnected to the second bond pad, the first and second bond pads functional to a receive and respond to an operational mode signals by entering an operational mode.

33. The bond pad structure of Claim 32, wherein the lower metal layer of the first bond pad extends underneath the upper metal layer of the second bond pad.

34. The bond pad structure of Claim 32, wherein the lower metal layer of the second bond pad extends underneath the upper metal layer of the first bond pad.

~~35. A method of forming a bond pad structure comprising a first and second bond pad, the method comprising the steps of:~~

~~depositing a first metal layer onto a substrate;~~

~~etching the first metal layer to form first and second lower metal layers having a space thereinbetween;~~

~~depositing a dielectric layer over the first and second lower metal layers and into the space thereinbetween;~~

~~etching the dielectric layer to form openings to each of the first and second lower metal layers;~~

~~depositing a second metal layer over the dielectric layer and into the openings of the dielectric layer; and~~

~~etching the second metal layer to form first and second upper metal layers having a space thereinbetween; the first upper metal layer overlying the first lower metal layer to form a first bond pad, and the second upper metal layer overlying the second lower metal layer to form a second bond pad;~~

~~wherein the lower metal layer of one of the bond pads extends underneath the upper layer of the other of the bond pads.~~

~~36. The method of Claim 35, further comprising:~~

~~forming a passivation layer over the first and second upper metal layers and into the space thereinbetween; and~~

~~etching the passivation layer to form an opening to expose the first and second upper metal layers of the bond pads;~~

~~wherein the extension of the lower metal layer of the one bond pad functions as an etch block to prevent etching of the dielectric material between the first and second bond pads to the substrate underlying the bond pads.~~

~~37. The method of Claim 35, further comprising connecting the first and second bond pads with a conductive material.~~

~~38. The method of Claim 37, wherein the step of connecting the bond pads comprises depositing the conductive material as a layer over at least a portion of each of the first and second bond pads.~~

~~39. The method of Claim 37, wherein the conductive material comprises a solder material.~~

~~40. The method of Claim 37, further comprising connecting a bonding wire to the conductive material.~~

~~41. The method of Claim 35, wherein the step of etching the first metal layer comprises patterning and etching the first metal layer whereby the lower metal layer of the first bond pad extends underneath the upper metal layer of the second bond pad.~~

~~42. The method of Claim 35, wherein the step of etching the first metal layer comprises patterning and etching the first metal layer whereby the lower metal layer of the second bond pad extends underneath the upper metal layer of the first bond pad.~~

~~43. The method of Claim 35, wherein each of the lower metal layers comprise two or more metal layers.~~

~~44. A method of forming a bond pad structure comprising a first and second bond pad, the method comprising the steps of:~~

~~depositing a first metal layer onto a substrate;~~

~~etching the first metal layer to form first and second lower metal layers having a space thereinbetween;~~

~~depositing a dielectric layer over the first and second lower metal layers and into said space thereinbetween;~~

~~etching the dielectric layer to form openings to each of the first and second lower metal layers;~~

~~depositing a second metal layer over the dielectric layer and into the openings of the dielectric layer;~~

~~etching the second metal layer to form first and second upper metal layers having a space thereinbetween; the first upper and lower metal layers comprising a first bond pad, and the second upper and lower metal layers comprising second bond pad;~~

~~forming a passivation layer over the first and second bond pads; and~~

~~etching the passivation layer to form an opening to expose the first and second bond pads;~~

~~wherein the step of etching the first metal layer comprises patterning and etching the first metal layer whereby the lower metal layer of one bond pad extends underneath the upper metal layer of the other bond pad and functions as an etch block during the step of etching the passivation layer to prevent etching of the dielectric material between the first and second bond pads to the substrate underlying the bond pads.~~

~~45. The method of Claim 44, wherein the step of etching the first metal layer comprises patterning and etching the first metal layer whereby the lower metal layer of the first bond pad extends underneath the upper metal layer of the second bond pad.~~

~~46. The method of Claim 44, wherein the step of etching the first metal layer comprises patterning and etching the first metal layer whereby the lower metal layer of the second bond pad extends underneath the upper metal layer of the first bond pad.~~

~~47. The method of Claim 44, further comprising, after the passivation etching step, the step of connecting the first and second bond pads with a conductive material.~~

~~48. The method of Claim 47, wherein the step of connecting the bond pads comprises depositing the conductive material as a layer over at least a portion of each of the first and second bond pads.~~

~~49. The method of Claim 47, further comprising, connecting a bonding wire to the conductive material.~~

50. An integrated circuit die, comprising:

a first bond pad and a second bond pad, the first and second bond pads being positioned within a single passivation opening; each of the first and second bond pads comprising at least a lower metal layer and an upper metal layer; with a lower metal layer of one of the bond pads extending underneath the upper metal layer of the other of the bond pads.

51. The integrated circuit die of Claim 50, wherein the lower metal layer of the first bond pad extends underneath the upper metal layer of the second bond pad.

52. The integrated circuit die of Claim 50, wherein the lower metal layer of the second bond pad extends underneath the upper metal layer of the first bond pad.

53. The integrated circuit die of Claim 50, further comprising a conductive material interconnecting and overlying at least a portion of the first bond pad and the second bond pad.

54. The integrated circuit die of Claim 53, wherein the conductive material comprises solder.

55. The integrated circuit die of Claim 53, further comprising a bonding wire connected to at least one of the bond pads.

56. The integrated circuit die of Claim 50, wherein the first and second bond pads each comprise a plurality of lower metal layers wherein at least two lower metal layer of the one of the bond pads extend underneath the upper metal layer of the other of the bond pads.

57. The integrated circuit die of Claim 50, wherein the extension of the lower metal layer of the one of the bond pads functions as an etch block to prevent etching of a dielectric material between the first and second bond pads to a substrate underlying the bond pads.

58. An integrated circuit die, comprising:

a first bond pad interconnected to a second bond pad, the first and second bond pads being positioned within a single passivation opening;

each of the first and second bond pads comprising at least a lower metal layer and an upper metal layer; with a lower metal layer of one of the bond pads extending beneath the upper metal layer of the other of the bond pads; wherein the extension of the lower metal layer of the one of the bond pads functions as an etch block to prevent etching of a dielectric layer between the first and second bond pads to a substrate underlying the bond pads.

59. The integrated circuit die of Claim 58, wherein the first and second bond pads are interconnected by a conductive material interconnecting overlying and in conductive contact with at least a portion of each of the bond pads.

60. An integrated circuit die, comprising:

a first bond pad interconnected to a second bond pad, the first and second bond pads being positioned within a single passivation opening; each of the first and second bond pads comprising at least a lower metal layer and an upper metal layer; and the lower metal layer of the first bond pad extending beneath the upper metal layer of the second bond pad.

61. An integrated circuit die, comprising:

a first bond pad interconnected to a second bond pad, the first and second bond pads being positioned within a single passivation opening; each of the first and second bond pads

comprising at least a lower metal layer and an upper metal layer; with the lower metal layer of the second bond pad extending beneath the upper metal layer of the first bond pad.

62. An integrated circuit die, comprising:

a first bond pad and a second bond pad; each of the first and second bond pads comprising at least a lower metal layer and an upper metal layer; the lower metal layer of one of the bond pads extending beneath the upper metal layer of the other of the bond pads; and at least one of the bond pads functional to supply data, retrieve data, test a device, or supply various voltages.

63. The integrated circuit die of Claim 62, further comprising a conductive material interconnecting and overlying at least a portion of each of the bond pads.

64. The integrated circuit die of Claim 62, wherein the first bond pad is functional to receive and respond to a test mode signal by entering a test mode, and upon discontinuing the test mode and being interconnected to the second bond pad, the first and second bond pads are functional to receive and respond to an operational mode signal by entering an operational mode.

65. The integrated circuit die of Claim 64, further comprising a conductive material interconnecting and overlying at least a portion of each of the bond pads.

~~66. A method of testing and operating an integrated circuit, comprising the steps of:~~

~~providing an integrated circuit die comprising a first bond pad and a second bond pad; the bond pads being unconnected and within a single passivation opening; each of the bond pads comprising at least a lower metal layer and an upper metal layer; with a lower metal layer of one of the bond pads extending underneath the upper metal layer of the other of the bond pads; the first bond pad functional to receive and respond to a test mode signal by entering a test mode, and upon discontinuing the test mode and being connected to the second bond pad,~~

~~the first and second bond pads are functional to receive and respond to an operational mode signal by entering an operational mode;~~

~~signaling the first bond pad with the test mode signal to enter the test mode to test the integrated circuit die;~~

~~upon completion of the testing of the die, interconnecting the first and second bond pads with a conductive material; and~~

~~signaling the first and second bond pads with an operational mode signal to enter an operational mode.~~

~~67. The method of Claim 66, wherein the first bond pad is connected to the second bond pad with a solder material.~~

~~68. The method of Claim 66, further comprising, prior to the second signaling step, connecting a bonding wire to the conductive material.~~

69. (new) A bond pad structure disposed on a substrate and comprising multiple bond pads, each bond pad comprising overlying upper and lower metal layers, and the upper metal layer of one of the bond pads overlapping the lower metal layer of another of the bond pads.

70. (new) A bond pad structure disposed on a substrate and comprising two or more bond pads, each bond pad comprising overlying upper and lower metal layers, and the upper metal layer of one of the bond pads extending over the lower metal layer of another of the bond pads.

71. (new) A bond pad structure disposed on a substrate and comprising:

a lower metal layer disposed on the substrate and comprising first and second portions separated by a space therebetween;

a dielectric layer overlying the lower metal layer and the substrate within the space; one or more openings extending through the dielectric layer to each of the first and second lower metal portions; and

an upper metal layer disposed over the dielectric layer and within the openings in the dielectric layer in contact with the first and second portions of the lower metal layer; the upper metal layer comprising first and second portions, the first upper metal portion positioned over the first lower metal portion to form a first bond pad, and the second upper metal portion positioned over the second lower metal portion to form a second bond pad; and the upper metal portion of one of the bond pads extends over the lower metal portion of the other bond pad.

72. (new) An integrated circuit supported by a substrate and comprising: a bond pad structure, the bond pad structure comprising two or more bond pads, each bond pad comprising overlying upper and lower metal layers, and the upper metal layer of one of the bond pads extending over the lower metal layer of another of the bond pads.

73. (new) An integrated circuit supported by a substrate and comprising: a first bond pad and a second bond pad; each of the bond pads comprising a lower metal layer and an overlying upper metal layer; and the upper metal layer of one of the bond pads extends beyond the lower metal layer of the one bond pad and over the lower metal layer of the other of the bond pads.

74. (new) An integrated circuit supported by a substrate and comprising a bond pad structure, the bond pad structure comprising:

a lower metal layer comprising first and second portions with a space therebetween;

a dielectric layer overlying the lower metal layer and within the space; at least one opening extending through the dielectric layer to each of the first and second lower metal portions; and

an upper metal layer overlying the dielectric layer and within the openings in the dielectric layer in contact with the first and second portions of the lower metal layer; the upper metal layer comprising first and second portions, the first upper metal portion positioned over the first lower metal portion to form a first bond pad, and the second upper metal portion positioned over the second lower metal portion to form a second bond pad; and the upper metal portion of one of the bond pads extends over the lower metal portion of the other bond pad.

75. (new) A semiconductor device, comprising:

a substrate; and

a bond pad structure disposed on the substrate, the bond pad structure comprising multiple bond pads, each bond pad comprising overlying upper and lower metal layers, and the upper metal layer of one of the bond pads overlaps the lower metal layer of another of the bond pads.

76. (new) A semiconductor wafer, comprising:

a substrate and a bond pad structure disposed on the substrate, the bond pad structure comprising a first bond pad and a second bond pad; each of the bond pads comprising a lower metal layer and an overlying upper metal layer; and the upper metal layer of one of the bond pads extends beyond the lower metal layer of the one bond pad and over the lower metal layer of the other of the bond pads.